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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,574	08/16/2001	Rodrigo Cordero	S1022/8733	2206

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EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,574	CORDERO, RODRIGO	
	Examiner	Art Unit	
	Joseph Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 and 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Higuchi et al., Japanese Patent JP 04292018 A, hereinafter referred to as "Higuchi".

3. An English abstract was provided along with JP 04292018 A in the previous Office Action.

4. A full English Translation is provided for JP 0429018 A in this office action, references to these three documents will be collectively referred to as "Higuchi".

5. Referring to claim 1, Higuchi teaches a CRC circuit for checking errors based on polynomials, interpreted as mathematical functions (See Fig. 1 and 2, and abstract).

Higuchi discloses a circuit with an input stage that receives input data and feedback data (See Fig. 1 and 2). Also disclosed is a plurality of flip-flips, this is interpreted collectively as a register, to store data at input nodes and to selectively supply feedback to the input stage (See Fig. 1 and 2, and abstract). Higuchi teaches the circuit having

selectors, also known as multiplexing circuitry, that for both routing the feedback to the data input and for connecting the error circuitry to perform variable CRC checks (See Fig. 1 and 2, and abstract).

6. Referring to claim 2, Higuchi teaches the register being composed of flip-flops, this is interpreted as a plurality of delay elements, each being capable of holding one bit (See Fig. 1 and 2, and abstract).

7. Referring to claim 3, Higuchi discloses a first data input node and a selectable input node at every flip-flop of the register (See Fig. 1 and 2).

8. Referring to claims 9 and 11, Higuchi teaches the circuitry have 1 to n stages, this is interpreted to include a 16-bit and 32-bit CRC generator polynomials (See Fig. 1 and paragraph 0009 on page 4 of translation).

9. Referring to claim 10, Higuchi teaches transmitting data, this is interpreted as digital video data stream (See paragraph 0001 on page 2 of translation).

10. Referring to claim 12, Higuchi teaches a circuit that provides the method of checking an inputted bits stream for errors using a CRC function (See abstract). An input stage receives the incoming bit stream. A plurality flip-flops form a register that receive a plurality of input signal that are can select to receive the input signal and

generate a plurality of feedback signals (See Fig. 1 and 2). Higuchi also discloses the being able to connect the feedback signal to the input stage to perform an error check based on a CRC polynomial, which is interpreted as a mathematical function (See Fig. 1 and 2, and abstract). Higuchi finally teaches the CRC circuit being variable and thus can be rearranged to perform a second different CRC function (See abstract).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi in view of Erickson et al., U.S. Patent 5,598,424, hereinafter referred to as "Erickson et al".

13. Referring to claim 4, Higuchi teaches all the limitations (See rejection of claim 3) including the multiplexing circuitry arranged to selectively connect an incoming data signal from the input stage to said data input nodes of the register (See Fig. 1 and 2, and abstract). Higuchi does not teach the multiplexing circuitry also inputting a zero signal to the data input node, however Higuchi does disclose the multiplexing circuitry selecting between output of the previous flip-flop and the input signal XORed with the output of the previous flip-flop. This arrangement provides the same result for the same

purpose as the claimed arrangement. Erickson teaches error detection using polynomials. Erickson discloses multiplexing circuitry that selects between an input signal and a zero signal to be connected to the input signal of the register (See Fig. 6 and Col. 8, lines 54-60). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the multiplexing circuitry of Erickson in place of the multiplexing circuitry Higuchi. This would have been obvious to one of ordinary skill in the art at the time of the invention to do this because the two circuits are functional the same providing same result for the same purpose.

14. Referring to claims 5-7, Higuchi and Erickson discloses all the limitations (See rejection of claims 1-4) including the multiplexing circuitry having combinatorial logic for combining the incoming data with a feedback signal from the register. Higuchi teaches the use of a XOR gate for combining the signals (See Fig. 1 and 2, and abstract). Higuchi teaches the combinatorial and multiplexing circuitry having two stages, one that controls the feedback to the initial data input and a second one that controls the input data going to the remainder of the flip-flops of the register (See Fig. 1 and 2, and abstract).

~~15. Referring to claim 8 Higuchi and Erickson teach all the limitations (See rejection~~ of claim 7), including a multiplexor select signal that indicates the mathematical function to be used is being supplied to both stages. Higuchi teaches a decoder that has a

select line to the multiplexors that is used to generate the CRC function (See Fig. 1 and 2, and abstract).

Response to Arguments

16. Applicant's arguments, see page 6 of amendment, filed 23 July 2004, with respect to the specification have been fully considered and are persuasive. The objection of the specification has been withdrawn.

17. Applicant's arguments, see page 6 of amendment, filed 23 July 2004, with respect to claims 9, 10, and 11 have been fully considered and are persuasive. The objection of claims 9, 10, and 11 has been withdrawn.

18. Applicant's arguments filed 23 July 2004, with respect to the rejection of claims 1-8, and 12 have been fully considered but they are not persuasive.

Concerning the applicants arguments with respect to claim 1, the applicants states "Higuchi does not teach or suggest at least a plurality of input feedback nodes recited in claim 1". The examiner respectfully disagrees. Higuchi teaches the selector 40 having multiple inputs coming from every stage of the circuit (See Fig 2). It is interpreted as the selector being part of the data input stage and thus a plurality of input feedback nodes.

The applicants second argument concerning claim 1 is that Higuchi does not teach multiplexing circuitry that allows selectively connecting the data node to at least

some of the data input nodes. The examiner again respectfully disagrees. In Fig. 2 Higuchi shows selector, or "multiplexer" 40 as selecting the data input for the flip-flops, which collectively is interpreted as a register, and Higuchi shows multiplexers 13_1 to 13_7 being used to selectively connect the input to the data nodes.

Concerning the applicants arguments with respect to claim 12, the applicant uses the same arguments from claim 1. The examiner respectfully disagrees with these arguments. See above response to arguments.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
October 13, 2004

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